CLAIMS

What is claimed is:

1. A decoder that updates a plurality of edge messages using min†- (min-dagger minus) processing when decoding an LDPC (Low Density Parity Check) coded signal, the decoder comprising:

an m-bit symbol metric computer functional block that calculates a plurality of m-bit symbol metrics that correspond to a symbol of the LDPC coded signal wherein the symbol has m-bits and wherein the LDPC coded signal includes a plurality of symbols;

a symbol node calculator functional block that calculates a plurality of bit metrics using the plurality of m-bit symbol metrics;

a bit node calculator functional block that computes soft messages corresponding to the m-bits of the symbol using the plurality of bit metrics;

a check node operator functional block that provides a plurality of edge messages to the bit node calculator functional block;

wherein the plurality of edge messages corresponds to a plurality of edges that communicatively couple a plurality of bit nodes to a plurality of check nodes within an LDPC bipartite graph that corresponds to an LDPC code by which the LDPC coded signal is generated;

wherein the bit node calculator functional block updates the plurality of edge messages provided from the check node operator functional block using the plurality of bit metrics calculated by the symbol node calculator functional block;

wherein the bit node calculator functional block performs min†- processing when updating the plurality of edge messages;

wherein the bit node calculator functional block provides the updated plurality of edge messages to the check node operator functional block while the bit node calculator functional block updates the soft messages corresponding to the m-bits of the symbol using the updated plurality of edge messages; and

wherein the bit node calculator functional block and the check node operator functional block operate cooperatively to perform iterative decoding and to output best

estimates of the m-bits of the symbol of the LDPC coded signal using latest updated soft messages corresponding to the m-bits of the symbol of the LDPC coded signal.

2. The decoder of claim 1, wherein:

wherein, during a last iterative decoding iteration, the bit node calculator functional block makes a best estimate for the symbol of the LDPC coded signal using that symbol's most recently updated soft messages; and

further comprising:

a hard limiter that makes bit estimates based on the best estimate for the symbol of the LDPC coded signal such that the bit estimates are hard decisions for each of the individual bits of the symbol.

3. The decoder of claim 1, further comprising:

a syndrome calculator that determines whether each syndrome of a plurality of syndromes associated with the LDPC code is substantially equal to zero as defined by a predetermined degree of precision during each iterative decoding iteration; and

when, during a given iterative decoding iteration, the syndrome calculator determines that each of the syndromes of the plurality of syndromes associated with the LDPC code is substantially equal to zero as defined by the predetermined degree of precision, then the syndrome calculator determines that the given iterative decoding iteration is the last iterative decoding iteration.

4. The decoder of claim 1, wherein:

the updating of the updating the plurality of edge messages that is performed by the bit node calculator functional block is mathematically performed in the logarithmic domain using the min†- processing;

the bit node calculator functional block includes a min†- processing functional block to perform the min†- processing when updating the plurality of edge messages;

the min†- processing functional block performs min*- (min-star minus) processing on at least 2 input values;

when the results of the min*- processing on the at least 2 input values is not substantially greater than zero, then the min†- processing functional block outputs a zero valued output; and

when the results of the min*- processing on the at least 2 input values is substantially greater than zero, then the min†- processing functional block outputs a result generated by the min*- processing on the at least 2 input values.

5. The decoder of claim 4, wherein:

the bit node calculator functional block includes a min*- processing functional block to perform the min*- processing on the at least 2 input values;

the min*- processing functional block determines a minimum value among the at least 2 input values;

the min*- processing functional block calculates a logarithmic correction factor using the at least 2 input values; and

the min*- processing functional block combines the minimum value and the logarithmic correction factor to generate the result of the min*- processing on the at least 2 input values.

6. The decoder of claim 1, wherein:

the bit node calculator functional block selectively performs min†- processing when updating edge messages within the plurality of edge messages that are not indexed by a minimal index; and

the bit node calculator functional block selectively assigns edge messages within the plurality of edge messages that are indexed by the minimal index to a predetermined value.

7. The decoder of claim 1, wherein:

the bit node calculator functional block selectively performs min†- processing when updating edge messages within the plurality of edge messages that are not indexed by a minimal index; and

the bit node calculator functional block selectively assigns edge messages within the plurality of edge messages that are indexed by the minimal index to a predetermined value.

8. The decoder of claim 1, wherein:

the LDPC coded signal is a variable modulation signal;

a first symbol of the plurality of symbols is mapped according to a first modulation that includes a first constellation and a corresponding first mapping; and

a second symbol of the plurality of symbols is mapped according to a second modulation that includes a second constellation and a corresponding second mapping.

9. The decoder of claim 8, wherein:

the first modulation includes an 8 PSK (8 Phase Shift Key) shaped constellation whose constellation points are mapped according to the first mapping; and

the second modulation includes the 8 PSK shaped constellation whose constellation points are mapped according to the second mapping.

10. The decoder of claim 1, wherein:

the LDPC coded signal is a variable code rate signal;

a first symbol of the plurality of symbols is encoded according to a first code rate; and

a second symbol of the plurality of symbols is encoded according to a second code rate.

11. The decoder of claim 1, wherein:

the decoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point radio communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, a fiber-

optic communication system, a WLAN (Wireless Local Area Network) communication system, and a DSL (Digital Subscriber Line) communication system.

12. A decoder that is operable to perform min†- (min-dagger minus) processing when decoding an LDPC (Low Density Parity Check) coded signal, the decoder comprising:

a bit node calculator functional block that updates a plurality of edge messages provided from a check node operator functional block using a plurality of bit metrics;

wherein the bit node calculator functional block performs min†- processing when updating the plurality of edge messages;

wherein the updating of the updating the plurality of edge messages that is performed by the bit node calculator functional block is mathematically performed in the logarithmic domain using the min†- processing;

wherein the bit node calculator functional block includes a min†- processing functional block to perform the min†- processing when updating the plurality of edge messages;

wherein the min†- processing functional block performs min*- (min-star minus) processing on at least 2 input values;

wherein, when the results of the min*- processing on the at least 2 input values is not substantially greater than zero, then the min†- processing functional block outputs a zero valued output; and

wherein, when the results of the min*- processing on the at least 2 input values is substantially greater than zero, then the min†- processing functional block outputs a result generated by the min*- processing on the at least 2 input values.

13. The decoder of claim 12, wherein:

the bit node calculator functional block includes a min*- processing functional block to perform the min*- processing on the at least 2 input values;

the min*- processing functional block determines a minimum value among the at least 2 input values;

the min*- processing functional block calculates a logarithmic correction factor using the at least 2 input values; and

the min*- processing functional block combines the minimum value and the logarithmic correction factor to generate the result of the min*- processing on the at least 2 input values.

14. The decoder of claim 12, wherein:

the bit node calculator functional block selectively performs min†- processing when updating edge messages within the plurality of edge messages that are not indexed by a minimal index; and

the bit node calculator functional block selectively assigns edge messages within the plurality of edge messages that are indexed by the minimal index to a predetermined value.

15. The decoder of claim 12, wherein:

the LDPC coded signal is a variable modulation signal that includes a plurality of symbols;

a first symbol of the plurality of symbols is mapped according to a first modulation that includes a first constellation and a corresponding first mapping; and

a second symbol of the plurality of symbols is mapped according to a second modulation that includes a second constellation and a corresponding second mapping.

16. The decoder of claim 15, wherein:

the first modulation includes an 8 PSK (8 Phase Shift Key) shaped constellation whose constellation points are mapped according to the first mapping; and

the second modulation includes the 8 PSK shaped constellation whose constellation points are mapped according to the second mapping.

17. The decoder of claim 12, wherein:

the LDPC coded signal is a variable code rate signal that includes a plurality of symbols;

a first symbol of the plurality of symbols is encoded according to a first code rate; and

a second symbol of the plurality of symbols is encoded according to a second code rate.

18. The decoder of claim 12, wherein:

the decoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point radio communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, a fiber-optic communication system, a WLAN (Wireless Local Area Network) communication system, and a DSL (Digital Subscriber Line) communication system.

19. A decoder that is operable to perform min†- (min-dagger minus) processing when decoding an LDPC (Low Density Parity Check) coded signal, the decoder comprising:

a min†- processing functional block that includes a min*- processing functional block that performs min*- (min-star minus) processing on at least 2 input values;

wherein, when the results of the min*- processing on the at least 2 input values is not substantially greater than zero, then the min†- processing functional block outputs a zero valued output;

wherein, when the results of the min*- processing on the at least 2 input values is substantially greater than zero, then the min†- processing functional block outputs a result generated by the min*- processing on the at least 2 input values;

wherein the min*- processing functional block determines a minimum value among the at least 2 input values;

wherein the min*- processing functional block calculates a logarithmic correction factor using the at least 2 input values; and

wherein the min*- processing functional block combines the minimum value and the logarithmic correction factor to generate the result of the min*- processing on the at least 2 input values.

20. The decoder of claim 19, wherein:

the min†- processing functional block is included within a bit node calculator functional block that updates a plurality of edge messages provided from a check node operator functional block using a plurality of bit metrics;

the bit node calculator functional block performs min†- processing when updating the plurality of edge messages; and

the updating of the updating the plurality of edge messages that is performed by the bit node calculator functional block is mathematically performed in the logarithmic domain using the min†- processing.

21. The decoder of claim 20, wherein:

the bit node calculator functional block selectively performs min†- processing when updating edge messages within the plurality of edge messages that are not indexed by a minimal index; and

the bit node calculator functional block selectively assigns edge messages within the plurality of edge messages that are indexed by the minimal index to a predetermined value.

22. The decoder of claim 19, wherein:

the LDPC coded signal is a variable modulation signal that includes a plurality of symbols;

a first symbol of the plurality of symbols is mapped according to a first modulation that includes a first constellation and a corresponding first mapping; and

a second symbol of the plurality of symbols is mapped according to a second modulation that includes a second constellation and a corresponding second mapping.

23. The decoder of claim 22, wherein:

the first modulation includes an 8 PSK (8 Phase Shift Key) shaped constellation whose constellation points are mapped according to the first mapping; and

the second modulation includes the 8 PSK shaped constellation whose constellation points are mapped according to the second mapping.

24. The decoder of claim 19, wherein:

the LDPC coded signal is a variable code rate signal that includes a plurality of symbols;

a first symbol of the plurality of symbols is encoded according to a first code rate; and

a second symbol of the plurality of symbols is encoded according to a second code rate.

25. The decoder of claim 19, wherein:

the decoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point radio communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, a fiber-optic communication system, a WLAN (Wireless Local Area Network) communication system, and a DSL (Digital Subscriber Line) communication system.

26. A method for updating a plurality of edge messages using min†- (min-dagger minus) processing when decoding an LDPC (Low Density Parity Check) coded signal, the method comprising

receiving a plurality of edge messages with respect to a plurality of check nodes within an LDPC bipartite graph that corresponds to an LDPC code;

initializing a minimal absolute valued edge message of the plurality of the plurality of edge messages;

initializing a minimal index for the plurality of the plurality of edge messages;

initializing a sign function of a first edge message of the plurality of edge messages;

performing decoding processing across all other edge messages, besides the first edge message, of the plurality of edge messages that includes:

selectively replacing the minimal absolute valued edge message with an absolute value of a current edge message when the absolute value of the current edge message is substantially less than or equal with the minimal absolute valued edge message and updating the minimal index for the plurality of the plurality of edge messages;

computing min* (min-star) results of the absolute values of all edge messages of the plurality of edge messages except for the minimal absolute valued edge message;

computing a sign function of a current edge message using a sign function of a previous edge message, as defined according to the decoding processing;

computing min* results of absolute values of all edge messages of the plurality of edge messages; and

updating the plurality of edge messages with respect to a plurality of bit nodes within the LDPC bipartite graph that corresponds to the LDPC code using min†-processing.

27. The method of claim 26, further comprising:

selectively performing min†- processing when updating edge messages within the plurality of edge messages that are not indexed by the minimal index for the plurality of the plurality of edge messages; and

selectively assigning edge messages within the plurality of edge messages that are indexed by the minimal index to a predetermined value.

28. The method of claim 26, wherein:

the min†- processing performs min*- (min-star minus) processing on at least 2 input values;

when the results of the min*- processing on the at least 2 input values is not substantially greater than zero, then the min†- processing outputs a zero valued output;

when the results of the min*- processing on the at least 2 input values is substantially greater than zero, then the min†- processing outputs a result generated by the min*- processing on the at least 2 input values;

the min*- processing determines a minimum value among the at least 2 input values;

the min*- processing calculates a logarithmic correction factor using the at least 2 input values; and

the min*- processing combines the minimum value and the logarithmic correction factor to generate the result of the min*- processing on the at least 2 input values.

29. The method of claim 26, wherein:

the LDPC coded signal is a variable modulation signal that includes a plurality of symbols;

a first symbol of the plurality of symbols is mapped according to a first modulation that includes a first constellation and a corresponding first mapping; and

a second symbol of the plurality of symbols is mapped according to a second modulation that includes a second constellation and a corresponding second mapping.

30. The method of claim 29, wherein:

the first modulation includes an 8 PSK (8 Phase Shift Key) shaped constellation whose constellation points are mapped according to the first mapping; and

the second modulation includes the 8 PSK shaped constellation whose constellation points are mapped according to the second mapping.

31. The method of claim 26, wherein:

the LDPC coded signal is a variable code rate signal that includes a plurality of symbols;

a first symbol of the plurality of symbols is encoded according to a first code rate; and

a second symbol of the plurality of symbols is encoded according to a second code rate.

32. The method of claim 26, wherein:

the method is performed within a decoder;

the decoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point radio communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, a fiber-optic communication system, a WLAN (Wireless Local Area Network) communication system, and a DSL (Digital Subscriber Line) communication system.

33. A method for performing min†- (min-dagger minus) processing on at least 2 input values, the method comprising:

performing min*- (min-star minus) processing on at least 2 input values;

when the results of the min*- processing on the at least 2 input values is not substantially greater than zero, outputting a zero valued output;

when the results of the min*- processing on the at least 2 input values is substantially greater than zero, outputting a result generated by the min*- processing on the at least 2 input values;

wherein the min*- processing involves determining a minimum value among the at least 2 input values;

wherein the min*- processing involves calculating a logarithmic correction factor using the at least 2 input values; and

wherein the min*- processing involves combining the minimum value and the logarithmic correction factor to generate the result of the min*- processing on the at least 2 input values.

34. The method of claim 33, wherein:

the min†- processing is performed within a decoder that decodes an LDPC (Low Density Parity Check) coded signal;

the min†- processing is performed within a bit node calculator functional block of the decoder that updates a plurality of edge messages provided from a check node operator functional block of the decoder using a plurality of bit metrics;

the bit node calculator functional block performs min†- processing when updating the plurality of edge messages; and

the updating of the updating the plurality of edge messages that is performed by the bit node calculator functional block is mathematically performed in the logarithmic domain using the min†- processing.

35. The method of claim 34, further comprising:

selectively performing min†- processing when updating edge messages within the plurality of edge messages that are not indexed by a minimal index for the plurality of the plurality of edge messages; and

selectively assigning edge messages within the plurality of edge messages that are indexed by the minimal index to a predetermined value.